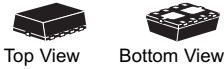




CTLDM8120-M832D

SURFACE MOUNT TLM™ DUAL, P-CHANNEL ENHANCEMENT-MODE SILICON MOSFETS



TLM832D CASE

APPLICATIONS:

- Switching Circuits
- DC/DC Converters
- Battery powered portable devices

MAXIMUM RATINGS: (T_A=25°C)

Drain-Source Voltage	
Gate-Source Voltage	
Continuous Drain Current (Steady State)	
Continuous Drain Current (t ≤ 5s)	
Continuous Source Current (Body Diode)	
Maximum Pulsed Drain Current (tp=10µs)	
Maximum Pulsed Source Current (tp=10µs)	
Power Dissipation*	
Operating and Storage Junction Temperature	
Thermal Resistance*	

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I _{GSSF}	V _{GS} =8.0V, V _{DS} =0V		1.0	50	nA
I _{GSSR}	V _{GS} =8.0V, V _{DS} =0V		1.0	50	nA
I _{DSS}	V _{DS} =20V, V _{GS} =0V		5.0	500	nA
BV _{DSS}	V _{GS} =0V, I _D =250µA	20	24		V
V _{GS(th)}	V _{DS} =V _{GS} , I _D =250µA	0.45	0.76	1.0	V
V _{SD}	V _{GS} =0V, I _S =360mA			0.9	V
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.95A		0.085	0.150	Ω
r _{DS(ON)}	V _{GS} =4.5V, I _D =0.77A		0.085	0.142	Ω
r _{DS(ON)}	V _{GS} =2.5V, I _D =0.67A		0.130	0.200	Ω
r _{DS(ON)}	V _{GS} =1.8V, I _D =0.2A		0.190	0.240	Ω
g _{fs}	V _{DS} =10V, I _D =810mA	2.0			S
C _{rss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		80		pF
C _{iss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		200		pF
C _{oss}	V _{DS} =16V, V _{GS} =0, f=1.0MHz		60		pF

*FR-4 Epoxy PCB with copper mounting pad area of 54mm²

Central™ Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLDM8120-M832D is an Enhancement-mode Dual P-Channel Field Effect Transistor, manufactured by the P-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. This MOSFET offers Low r_{DS(ON)} and Low Threshold Voltage.

MARKING CODE: CFV

FEATURES:

- Device is **Halogen Free** by design
- Device is **RoHS** compliant
- Low r_{DS(ON)} (0.24Ω MAX @ V_{GS}=1.8V)
- High current (I_D=0.95A)
- Logic level compatibility

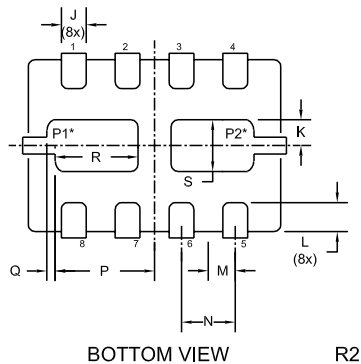
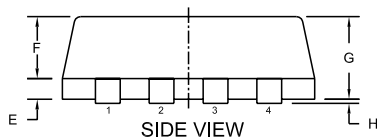
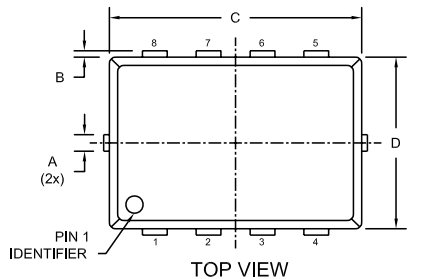
SYMBOL		UNITS
V _{DS}	20	V
V _{GS}	8.0	V
I _D	0.86	A
I _D	0.95	A
I _S	0.36	A
I _{DM}	4.0	A
I _{SM}	4.0	A
P _D	1.65	W
T _J , T _{stg}	-65 to +150	°C
θ _{JA}	76	°C/W

R0 (18-September 2008)

ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued:

SYMBOL	TEST CONDITIONS	TYP	UNITS
t_{on}	$V_{DD}=10V, V_{GS}=4.5V, I_D=950mA, R_G=6\Omega$	20	ns
t_{off}	$V_{DD}=10V, V_{GS}=4.5V, I_D=950mA, R_G=6\Omega$	25	ns

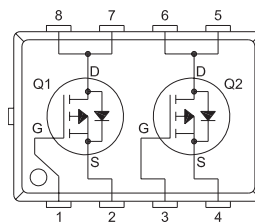
TLM832D CASE - MECHANICAL OUTLINE



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M	0.013		0.325	
N	0.026		0.650	
P	0.040	0.048	1.010	1.210
Q	0.004		0.100	
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

PIN CONFIGURATION



LEAD CODE:

- 1) GATE Q1
- 2) SOURCE Q1
- 3) GATE Q2
- 4) SOURCE Q2
- 5) DRAIN Q2
- 6) DRAIN Q2
- 7) DRAIN Q1
- 8) DRAIN Q1

MARKING CODE: CFV

*** Note:**

- Exposed pad P1 common to pins 7 and 8
- Exposed pad P2 common to pins 5 and 6